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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/743,919	12/24/2003	Hisashi Ishikawa	Q79066	9181

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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 02/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EK

Office Action Summary	Application No.	Applicant(s)	
	10/743,919	ISHIKAWA, HISASHI	
	Examiner	Art Unit	
	Jung (John) Hur	2824	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/7/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendment

1. Acknowledgment is made of applicant's Amendment, filed 17 November 2005. The changes and remarks disclosed therein have been considered.

No claims have been cancelled or added by Amendment. Therefore, claims 1-20 are pending in the application.

Information Disclosure Statement

2. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) Form PTO-1449, filed 07 November 2005. The information disclosed therein has been considered.

Specification

3. The amendment filed 17 November 2005 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Claims 12-14, as amended, now recites "a circuit board for interconnecting a plurality of different memory devices, each memory device having different packages or pin assignments to a motherboard," implying that memory devices with different packages or pin assignments are interconnected together, which appears to lack support in the original disclosure.

For the purpose of further examination on merits, said recitation will be understood as --a circuit board for interconnecting different memory device types, each memory device type having different packages or pin assignments to a motherboard--.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

4. Claims 12-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specifically, claims 12-14, as amended, now recites "a circuit board for interconnecting a plurality of different memory devices, each memory device having different packages or pin assignments to a motherboard," implying that memory devices with different packages or pin assignments are interconnected together, which appears to lack support in the original disclosure.

For the purpose of further examination on merits, said recitation will be understood as --a circuit board for interconnecting a plurality of memory device types, each memory device type having different packages or pin assignments to a motherboard--.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Delp et al. (U.S. Pat. No. 6,334,174) in view of Ozawa et al. (U.S. Pat. No. 6,483,772) and Solomon et al. (U.S. Pat. No. 6,681,293).

Regarding claim 1, Delp, for example in Figs. 5-7, discloses a semiconductor memory device comprising: a memory (76 in Fig. 5); and a memory control circuit (78 in Figs. 5 and 6) for controlling said memory, wherein: said memory control circuit comprises: a bank busy circuit for variably setting a bank busy time that controls different bank cycle times (related to, for example, "bank cycle time"; see column 7, lines 5-19 and Figs. 6 and 7); a read data input circuit having variable timing for inputting read data output from said memory (see column 7, lines 5-19 and Figs. 6 and 7 for various timing parameters); a write data output circuit having variable output timing for outputting write data to said memory (see column 7, lines 5-19 and Figs. 6 and 7 for various timing parameters); a command control circuit for issuing a command to said memory based on a memory command output from said bank busy circuit (for example, via 96 in Fig. 7); and an address generation circuit for controlling different address interfaces (88 through 82a, 82 and 84 in Fig. 6) (see for example column 10, lines 42-54 and column 11, lines 7-15).

Delp does not disclose a write mask circuit for controlling different write masks; and an initial sequence control circuit for controlling memories having different initial sequences.

Ozawa discloses a write mask circuit for controlling different write masks (Data Mask method and Variable Write burst length method; see for example column 1, lines 34-36, column 2, lines 4-22, and column 8, lines 39-47).

Solomon discloses an initial sequence control circuit for a memory (see for example column 27, line 39 through column 28, line 15).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include, in the device of Delp, a write mask circuit for controlling different write masks (as in Ozawa), for the purpose of providing a greater flexibility in accommodating additional types of memories, including high-speed memories, such as FCRAMs and DDRIIs (see for example Ozawa column 2, lines 4-14).

Further, since it was common and well known in the art to initialize a memory through an initial command sequence that would be unique to the memory (as exemplified in Solomon), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to additionally include, in the device of Delp, an initial sequence control circuit for controlling memories different in the initial sequence, for the purpose of reliably initializing a selected type of memory among various memory types.

Regarding claims 2 and 4, the above Delp/Ozawa/Solomon combination further discloses that said bank busy circuit comprises: a program register (94 in Figs. 6 and 7 of Delp) for variably setting the bank busy time; and a bank busy counter (98d in Fig. 7 of Delp) for setting a value set on said program register, and then counting down the set value for each clock cycle when a bank is accessed wherein said bank busy circuit provides said command control circuit

with a memory command indicating cleared bank busy when said set value of said bank busy counter becomes zero (see for example Delp column 12, lines 10-26 and 58-60);

wherein said bank busy circuit switches the bank busy time using a switch (see for example 84 in Fig. 6 and 98d in Fig. 7 of Delp).

Regarding claim 3, the above Delp/Ozawa/Solomon combination further discloses that: said read data input circuit comprises a first program register (as a part of 94 in Fig. 6 of Delp) for variably setting the input timing of the read data output from said memory, and inputting the read data output from said memory based on a variable input timing value set in the first program register, and said write data output circuit comprises a second program register (as a part of 94 in Fig. 6 of Delp) for variably setting the output timing of the write data output to said memory and adjusting the write data output timing based on a value set in the second program register (see for example Delp column 7, lines 5-19 and Figs. 6 and 7 for various timing parameters).

Regarding claims 5 and 6, the above Delp/Ozawa/Solomon combination further discloses that said write mask circuit comprises a program register (94 or 92, as modified in the above Delp/Ozawa/Solomon combination) or a switch (84, as modified in the above Delp/Ozawa/Solomon combination) for switching between masking a write operation using a Variable Write function when an FCRAM or an NWRAM is used, and masking the write operation using a Data Mask function when a DDR-SDRAM is used (see for example Ozawa column 2, lines 4-14, wherein DDR-SDRAM is distinguished from DDRIIs or DDR2s).

Regarding claims 7 and 8, the above Delp/Ozawa/Solomon combination further discloses that said address generation circuit (88 controlled by registers 90 in Fig. 6 of Delp) comprises a program register (94 in Fig. 6) or a switch (84 in Fig. 6) for switching address generation logic (via 82 and 82a in Fig. 6).

Regarding claims 9 and 10, the above Delp/Ozawa/Solomon combination further discloses that said initial sequence control circuit comprises a program register (94 or 92, as modified in the above Delp/Ozawa/Solomon combination) or a switch (84, as modified in the above Delp/Ozawa/Solomon combination) for variably changing the issue sequence of commands comprising mode register set (MRS), extension mode register set (EMRS), auto refresh, and all bank pre-charge, and for variably changing set values on a mode register and an extension mode register, and for issuing an initial sequence command comprising the mode register set (MRS), the extension mode register set (EMRS), the auto refresh, and the all bank pre-charge to said command control circuit (see for example Solomon column 27, line 39 through column 28, line 9).

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Delp et al. in view of Ozawa et al. and Solomon et al. as applied to claim 1 above, and further in view of Chang (U.S. Pat. No. 6,621,754)

The above Delp/Ozawa/Solomon combination discloses a semiconductor memory device as recited in claim 1, with the exception of a power supply capable of adjusting a power supply output level supplied for said memory.

Chang discloses a memory device comprising a power supply capable of adjusting a power supply output level supplied for a memory (see for example column 1, lines 59-67).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to include, in the device of the Delp/Ozawa/Solomon combination, a power supply capable of adjusting a power supply output level supplied for the memory (as in Chang), for the purpose of providing a greater flexibility in accommodating additional types of memories requiring different supply voltages (see for example Chang column 1, lines 59-67).

8. Claims 12-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Delp et al. in view of Ozawa et al. and Solomon et al. as applied to claims 1-3 above, and further in view of Doyle (U.S. Pat. No. 5,982,655).

The above Delp/Ozawa/Solomon combination discloses a semiconductor memory device as recited in claims 1-3, with the exception of a mount-type semiconductor device for mounting said semiconductor memory device comprising a circuit board for interconnecting a plurality of memory device types, each memory device type having different packages or pin assignments to a motherboard, wherein said interconnection between the motherboard and the circuit board has only one physical configuration; and wherein the board for mounting the memory thereon is a DIMM (Dual Inline Memory Module).

Doyle discloses a mount-type semiconductor device for mounting a semiconductor memory device comprising a circuit board (DIMM; see for example column 2, lines 9-15) for interconnecting a plurality of memory device types, each memory device type having different packages or pin assignments to a motherboard, wherein said interconnection between the

motherboard and the circuit board has only one physical configuration (see for example column 2, lines 9-15).

Since a DIMM configuration was common and well known in the art (as exemplified in Doyle), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to include, in the device of the Delp/Ozawa/Solomon combination, a means to support memories with different package sizes or pin assignments on a DIMM (as in Doyle), for the purpose of providing a greater flexibility in accommodating additional types of memories with various packages sizes or pin assignments (see for example Doyle column 2, lines 9-15).

9. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Delp et al. in view of Ozawa et al. and Solomon et al. as applied to claims 1-3 above, and further in view of Park et al. (U.S. Pat. No. 6,480,409).

The above Delp/Ozawa/Solomon combination discloses a semiconductor memory device as recited in claims 1-3, with the exception of a mount-type semiconductor device for mounting said semiconductor memory device on a circuit board for interconnecting said memory device on a motherboard, wherein: said circuit board comprises a DIMM (Dual Inline Memory Module), and a terminating resistor where said memory device does not comprise a terminating resistor; and said interconnection between the motherboard and the DIMM has only one phycial configuration.

Park disclose a memory device and a terminating resistor mounted on a DIMM (see for example Figs. 3, 4 and 7).

Since use of terminating resistors was common and well known in the art (as exemplified in Park), it would have been obvious at the time the invention was made to a person having ordinary skill in the art to mount a terminating resistor on a DIMM for memories that do not incorporate a terminating resistor while not mounting a terminating resistor for memories that do incorporate a terminating resistor, for the purpose of ensuring reduced noise and improved signal quality in a memory device that supports various types of memories, including those with or without a terminating resistor.

Response to Arguments

10. Applicant's arguments filed 17 November 2005 have been fully considered but they are not persuasive.

Regarding claim 1, Applicant argues, starting at the bottom of page 11, that:

> The portion of Delp cited by the Examiner, however, merely discloses a variety of timing characteristics relevant to different types of memory storage devices (col. 7, ll. 5-19). Delp discloses a tuning circuit 22 with a programmable delay counter 24 and a configuration register 26 which combine to insert programmable delays equivalent to a selected number of clock cycles between memory control operations (col. 7, ll. 19-33, 49-55). Memory control operations are implemented by a plurality of memory specific state machine/support logic blocks configured to implement various timing characteristics and protocols necessary for interfacing with different memory types (col. 10, ll. 45-54). Therefore, Delp discloses different circuit configurations necessary to read and write to different memory types. Delp does not, however, teach or suggest at least the singular read data input circuit or write data output circuit as recited in claim 1.

In response, it is note that Delp's memory control circuit includes, as quoted above, "a plurality of memory specific state machine/support logic blocks configured to implement various timing characteristics and protocols necessary for interfacing with different memory types (col. 10, ll. 45-54)" (emphasis added). This implies that, firstly, in order to interface with a memory,

Delp's memory control circuit includes a read data input circuit and a write data output circuit (also implied by the I/O signals in Figs. 6 and 7), and, secondly, in order to accommodate different memory types, said input and output circuits have variable input and output timings, respectively. Therefore, Delp does teach the input and output circuits as recited in claim 1.

Applicant further argues, in the middle paragraph on page 12, that:

> Ozawa discloses circuitry in a memory device that allows the memory device to be enabled for either the data mask method of masking data or the variable burst length method of masking data by either bonding or not bonding an inner lead to an option pad on the semiconductor chip (Figs. 1 , 3 and 10, and col. 5, ll. 1-11). Therefore, Ozawa teaches a mask circuit enabled by hard-wiring, not a circuit for controlling different write masks, as recited in claim 1.

In response, it is noted that Ozawa in Figs. 10 and 11 and starting at column 8, line 39 teaches an embodiment that includes a circuit that allows the user to select a data masking method, including among PDM and VWPDM methods in which the position for masking data is controlled. Therefore, Ozawa does teach a write mask circuit as recited in claim 1.

Applicant presents further arguments, staring at the bottom of page 12, with respect to claims 1-20, based on the above arguments for claim 1; however, in view of the above responses to the above arguments for claim 1, these further arguments are deemed moot.

In view of the above responses to Applicant's arguments and Applicant's statement on page 11 that claims "have been amended in a non-narrowing manner to correct grammatical and typographical errors unrelated to patentability," the previous rejections have been maintained with the amended claim language. See above rejections.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jung (John) Hur whose telephone number is (571) 272-1870. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jhh

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